**CLAIMS**:

1. A method of vertically stacking wafers, comprising:

selectively depositing a plurality of metallic lines on opposing surfaces of adjacent wafers;

bonding the adjacent wafers, via respective metallic lines on opposing surfaces of the adjacent wafers, to establish electrical connections between active devices on vertically stacked wafers; and

forming one or more vias to establish electrical connections between the active devices on the vertically stacked wafers and an external interconnect.

2. The method as claimed in claim 1, wherein each via is formed by:

selectively etching the top wafer to form a via;

depositing an oxide layer to insulate a sidewall of the via;

forming a barrier/seed layer in the via; and

depositing a conduction metal on the barrier/seed layer in the via for providing an electrical connection between active devices on the vertically stacked wafers and the external interconnect.

3. The method as claimed in claim 1, wherein the metallic lines are Copper (Cu)

lines deposited to serve as electrical contacts between active devices on the vertically stacked wafers.

4. The method as claimed in claim 2, wherein the conduction metal deposited in the via is copper (Cu) or a Cu alloy.

5. The method as claimed in claim 2, wherein the barrier/seed layer contains a barrier layer deposited in the via, and a copper (Cu) seed layer deposited in the trench overlying the barrier layer.

6. The method as claimed in claim 5, wherein the barrier layer is comprised of a material selected from one of the group including tantalum (Ta), tantalum nitride (TaN), titanium (Ti), and tungsten (W), and the Cu seed layer is comprised of a thin layer of copper (Cu) deposited on the barrier layer by chemical vapor deposition (CVD) process.

7. The method as claimed in claim 1, further comprising dummy vias arranged on opposing surfaces of the adjacent wafers to increase the surface area for wafer-to-wafer bonding and serve as auxiliary structures such as ground planes or heat conduits for the active devices on the vertically stacked wafers.

8. The method as claimed in claim 1, wherein the vias are formed tapered from the

top to the bottom via trench to increase the surface area for wafer to-wafer bonding in the adjacent wafers.

9. The method as claimed in claim 1, wherein each via is formed by a dual damascene process comprised of:

selectively etching the top wafer to form an upper trench section of a via;

depositing an oxide layer to insulate a sidewall of the upper trench section of the via;

selectively etching the oxide layer in the upper trench section of the via to form a lower trench section of the via;

depositing a barrier/seed layer in the upper trench section and the lower trench section of the via; and

depositing a conduction metal on the barrier/seed layer for providing an electrical connection between active devices on the vertically stacked wafers and an external interconnect.

10. The method as claimed in claim 9, wherein the barrier/seed layer includes a barrier layer comprised of a material selected from one of the group including tantalum (Ta), tantalum nitride (TaN), titanium (Ti), and tungsten (W), and deposited in the upper trench section overlying the oxide layer and the lower trench section of the via; and a copper (Cu) seed layer comprised of a thin layer of copper (Cu) deposited on the barrier layer, and deposited overlying the barrier layer in both the upper trench section and the lower trench section of the via.

11. The method as claimed in claim 1, wherein the vias are formed during a Shallow Trench Isolation (STI) process in the top wafer before the adjacent wafers are bonded, via the respective metallic lines deposited on opposing surfaces of the adjacent wafers.

12. A method of forming vertically stacked wafers, comprising:

depositing a plurality of metallic lines on opposing surfaces of top and bottom wafers;

forming a conductive plug;

bonding the adjacent wafers, via respective metallic lines, to form vertically stacked wafers; and

forming at least one via on the top wafer to establish electrical connections between the active devices on the vertically stacked wafers and an external interconnect, by selectively etching through the top wafer until stopped by the conductive plug, depositing an oxide layer to insulate a sidewall of the via, depositing a barrier/seed layer on the bottom of the via, and filling the via with a conduction metal to serve as electrical connections between active devices on the vertically stacked wafers and the external interconnect.

13. The method as claimed in claim 12, wherein the metallic lines are Copper (Cu) lines deposited to serve as electrical contacts between active devices on the vertically stacked wafers.

14. The method as claimed in claim 12, wherein the conduction metal deposited in the via is copper (Cu) or a Cu alloy.

15. The method as claimed in claim 12, wherein the barrier/seed layer contains a barrier layer deposited in the via, and a copper (Cu) seed layer deposited in the via overlying the barrier layer.

16. The method as claimed in claim 15, wherein the barrier layer is comprised of a material selected from one of the group including tantalum, titanium, and tungsten, and the Cu seed layer is comprised of a few layers of copper (Cu) atoms deposited on the barrier layer by chemical vapor deposition (CVD) process.

17. The method as claimed in claim 12, further comprising dummy vias arranged on opposing surfaces of the adjacent wafers to increase the surface area for wafer-to-wafer bonding and serve as auxiliary structures such as ground planes or heat conduits for the active devices on the vertically stacked wafers.

18. The method as claimed in claim 12, wherein the via is formed tapered from the top to the bottom via trench to increase the surface area for wafer to-wafer bonding in the adjacent wafers.

19. A three-dimensional (3-D) vertically stacked wafer system, comprising:

a first wafer including an active region to support one or more integrated circuit (IC) devices;

a second wafer including an active region to support one or more integrated circuit (IC) devices;

metallic lines deposited on opposing surfaces of the first and second wafers at designated areas to establish metal bonding between the first and second wafers in a stack and provide electrical connections between active IC devices on the first and second wafers in the stack; and

one or more vias formed, via the active region of the first wafer, to serve as electrical connections between the active IC devices on the first and second wafers in the stack and an external interconnect.

20. The three-dimensional (3-D) vertically stacked wafer system as claimed in claim 19, wherein the metallic lines include Copper (Cu) lines deposited on opposing surfaces of the first and second wafers to serve as electrical contacts between active IC devices on the first and second wafers.

21. The three-dimensional (3-D) vertically stacked wafer system as claimed in claim 20, wherein each via is formed by:

selectively etching the first wafer to form a via;

depositing an oxide layer to insulate a sidewall of the via;

forming a barrier/seed layer in the via; and

depositing a conduction metal on the barrier/seed layer in the via for providing an electrical connection between active IC devices on the vertically stacked wafers and the external interconnect.

22. The three-dimensional (3-D) vertically stacked wafer system as claimed in claim 21, wherein the conduction metal deposited in the via is copper (Cu) or a Cu alloy, and the barrier/seed layer includes a barrier layer deposited in the via overlying the oxide layer and a copper (Cu) seed layer deposited in the via overlying the barrier layer.

23. The three-dimensional (3-D) vertically stacked wafer system as claimed in claim 22, wherein the barrier layer is comprised of a material selected from one of the group including tantalum (Ta), tantalum nitride (TaN), titanium (Ti), and tungsten (W), and the Cu seed layer is comprised of a thin layer of copper (Cu) deposited on the barrier layer by chemical vapor deposition (CVD) process.

24. The three-dimensional (3-D) vertically stacked wafer system as claimed in claim 20, wherein each via is formed by a dual damascene process comprised of:

selectively etching the top wafer to form an upper trench section of the via;

depositing an oxide layer to insulate a sidewall of the upper trench section of the via;

etching the oxide layer in the upper trench section to form a lower trench section of the

via;

depositing a barrier/seed layer in the upper trench section and the lower trench section of the via; and

depositing a conduction metal on the barrier/seed layer for providing an electrical connection between active devices on the vertically stacked wafers and the external interconnect.

25. The three-dimensional (3-D) vertically stacked wafer system as claimed in claim 24, wherein the barrier/seed layer includes a barrier layer comprised of a material selected from one of the group including tantalum (Ta), tantalum nitride (TaN), titanium (Ti), and tungsten (W), and deposited in the upper trench section overlying the oxide layer and the lower trench section of the via; and a copper (Cu) seed layer comprised of a thin layer of copper (Cu) deposited on the barrier layer, and deposited overlying the barrier layer in both the upper trench section and the lower trench section of the via.

26. The three-dimensional (3-D) vertically stacked wafer system as claimed in claim 20, wherein the vias are formed during a Shallow Trench Isolation (STI) process in the first wafer before the first and second wafers are bonded, via the respective metallic lines deposited on opposing surfaces of the first and second wafers.

27. A three-dimensional (3-D) vertically stacked wafer system, comprising:

a first stack of wafers in which adjacent wafers are bonded, via metallic lines deposited

on opposing surfaces of the adjacent wafers at designated areas to establish metal bonding between the adjacent wafers and provide electrical connections between active IC devices on the adjacent wafers;

a first stack of wafers in which adjacent wafers are bonded, via metallic lines deposited on opposing surfaces of the adjacent wafers at designated areas to establish metal bonding between the adjacent wafers and provide electrical connections between active IC devices on the adjacent wafers; and

one or more vias formed on opposing surfaces of the first stack of wafers and the second stack of adjacent wafers to serve as electrical connections between the active IC devices on the first and second stacks of wafers and an external interconnect.

28. The three-dimensional (3-D) vertically stacked wafer system as claimed in claim 27, wherein the metallic lines include Copper (Cu) lines deposited on opposing surfaces of the adjacent wafers in the first and second stacks of wafers to serve as electrical contacts between active IC devices on the first and second stacks of wafers.

29. The three-dimensional (3-D) vertically stacked wafer system as claimed in claim 27, further comprising dummy vias arranged on opposing surfaces of the first and second stacks of adjacent wafers to increase the surface area for wafer-to-wafer bonding and serve as auxiliary structures such as ground planes or heat conduits for the active IC devices on vertically stacked wafers.

30. The three-dimensional (3-D) vertically stacked wafer system as claimed in claim 27, wherein the vias are formed tapered from the top to the bottom via trench to increase the surface area for wafer to-wafer bonding in the first and second stacks of adjacent wafers.

31. The three-dimensional (3-D) vertically stacked wafer system as claimed in claim 27, wherein each via is formed by a dual damascene process comprised of:

selectively etching the top wafer to form an upper trench section of a via;

depositing an oxide layer to insulate a sidewall of the upper trench section of the via;

etching the oxide layer in the upper trench section of the via to form a lower trench section of the via;

depositing a barrier/seed layer in the upper trench section and the lower trench section of the via; and

depositing a conduction metal on the barrier/seed layer for providing an electrical connection between active IC devices on the vertically stacked wafers and the external interconnect.

32. The three-dimensional (3-D) vertically stacked wafer system as claimed in claim 31, wherein the barrier/seed layer includes a barrier layer comprised of a material selected from one of the group including tantalum (Ta), tantalum (TaN), titanium (Ti), and tungsten (W), and deposited in the upper trench section overlying the oxide layer and the lower trench section of

the via; and a copper (Cu) seed layer comprised of a thin layer of copper (Cu) deposited on the barrier layer, and deposited overlying the barrier layer in both the upper trench section and the lower trench section of the via.